CMPE 443
Principles of Embedded System Design
fall'11

Problem Session
Overview

- Output Compare
  - General Info
  - Registers
- Input Capture
  - General Info
  - Registers
- Sample Code
Output Compare

- Used for more precise timing compared to the timer overflow interrupt

- PORT T can be controlled by the output compare functions or can be used for general Purpose I/O
Timer Input Capture/Output Compare Select

- Address: Base + $0040

Channel Configuration
- 0: The corresponding channel acts as input capture
- 1: The channel acts as output compare

When IOS[7:0] is zero, the PORT T can act as an I/O pin whose direction is controlled by register DDRT.
TCn

- Timer Input Capture/Output Compare Registers
  - 16-bit register for each channel (i.e., n=0–7)
Timer Interrupt Flag 1

- Address: Base+$004E

- Interrupt flag for the channels
- Used in the clearing process
  - Writing 1 clears the bit
Timer Interrupt Enable Register
- Address: Base+$004C

- Timer Interrupt Flags
  - 0: The corresponding bit in TFLG1 can not generate interrupt
  - 1: The corresponding bit in TFLG1 may generate an interrupt
Timer Control Register 1 & 2

- Addresses: Base+$0048 (TCTL1), Base+$0048 (TCTL2)

- OMn & OLn
  - 00: Timer disconnected from output pin logic (default)
  - 01: Toggle Ocn output line
  - 10: Clear Ocn output line to zero
  - 11: Set Ocn output line to 1
Timer System Control Registers

- Remember general timer system control registers
  - TSCR1
    - Address: Base+$0046
    - Set bit TEN to enable timer
  - TSCR2
    - Address: Base+$004D
    - Use bits PR2:PR1:PR0 to select the prescalar
Input Capture

- Latch the value of the free running counter TCNT in response to a program-selected, external signal from port T.
  - *Ex:* The length of a positive pulse can be measured by capturing the time at the rising edge and the again at the falling edge.
Timer Interrupt Enable Register

- Address: Base+$004C

Timer Interrupt Flags
- 0: The corresponding bit in TFLG1 cannot generate an interrupt
- 1: The corresponding bit in TFLG1 may generate an interrupt
Timer Control Register 3 & 4

- Addresses: Base+$004A (TCTL3), Base+$004B (TCTL4)

- EDGnB & EDGnA
  - 00: Capture Disabled (default)
  - 01: Capture on rising edges only
  - 10: Capture on falling edges only
  - 11: Capture on any edge (falling or rising)